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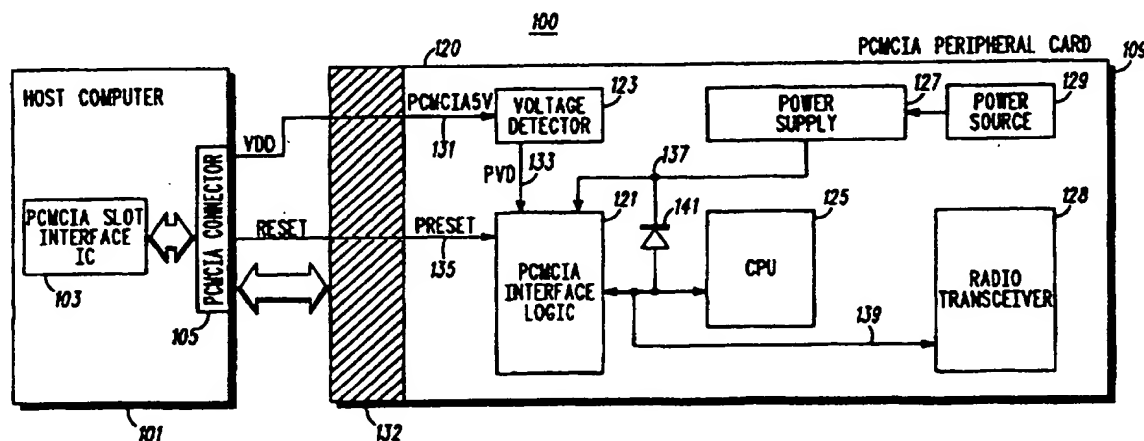
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(54) Title: A PERIPHERAL CARD HAVING INDEPENDENT FUNCTIONALITY AND METHOD USED THEREWITH



(57) Abstract

A PCMCIA card having independent functionality and alternatively arranged to operate in conjunction with a host computer, that includes a peripheral apparatus (109) having an integral CPU (125), a power source (129), and a power supply (127) for exhibiting an independent operating state; and an interface function (121) integral with and coupled to said peripheral apparatus (109), said interface function arranged and constructed to couple said peripheral apparatus to the host computer (101) over a PCMCIA compliant interface and initiate a dependent operating state at said peripheral apparatus (109).

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An Peripheral Card Having Independent Functionality and Method Used Therewith

Field Of The Invention

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This disclosure deals with peripheral functionality arranged and constructed to interface to a host computer and more specifically but not limited to independent functionality in the form of peripheral cards having a Personal Computer Memory Card International Association (PCMCIA) compliant interface arranged to operate in
10 conjunction with the host computer .

Background Of The Invention

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General and special purpose host computers often include provisions for various peripheral functionality, such as a communications modem, memory expansion, or an add on hard disk drive. In order to facilitate the addition of various peripherals the Personal Computer Memory Card International Association (PCMCIA)
20 has endeavored to standardize a family of peripheral cards with a requisite PCMCIA interface. The PCMCIA defined parameters can be found in the PC Card Standard Release 2.0 document, published by the PCMCIA, 1030B East Duane Avenue, Sunnyvale California and incorporated herein by reference. The defined parameters include
25 physical parameters such as dimensions, input/output connections such as control, address, and data buses, signal parameters such as operating levels, and impedances, power levels, source polarity and levels and certain operating procedures.

Based upon the provisions supported by the host computer
30 for additional devices such as the PCMCIA devices it is generally known that PCMCIA peripheral cards draw their power from the host computer socket and are generally controlled by a single RESET line when inserted or removed from the host computer socket in order to reinstate functionality.

However, a new class of PCMCIA devices, such as wireless modems, and the like, available from manufacturers such as Motorola, Inc. at 1303 East Algonquin Road, Schaumburg, Illinois 60193, are designed to continue to operate while removed from the socket or while the socket and the host computer are powered-off. These PCMCIA devices have their own power source and CPU that allows each device to maintain independent functionality once removed from the host computer socket. This paradigm shift allows the users the enhanced capabilities of remaining logged into a network while removed from the host computer thus operating in a manner that allows them to maintain a partial communication link such as, for example storing messages until the peripheral card is reinserted into the host computer.

However since existing PCMCIA peripheral cards, are designed to function in accordance with the PCMCIA standard where the only power source and reset state is generated by the host computer, an undesirable phenomenon can occur. This phenomenon results in the circuitry on the peripheral cards being unnecessarily or inadvertently reset, thus interfering with the planned or expected functionality of the device.

Clearly a need exists for a peripheral function or card that has a PCMCIA compliant interface that is additionally capable of operating reliably in a deterministic fashion in an environment where the host device and peripheral device both contain their own CPU and power source.

Brief Description Of The Drawings

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims. However, the invention together with further advantages thereof, may best be understood by reference to the accompanying drawings wherein:

FIG. 1 is a block diagram of a host computer and peripheral card suitable for employing a preferred embodiment in accordance with the instant invention;

FIG. 2 is a detailed block diagram of the peripheral card of FIG. 1.

FIG. 3 flowchart diagram of the steps performed at the peripheral card for determining whether the peripheral card is in a dependent or independent operating state.

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Detailed Description Of A Preferred Embodiment

Generally this disclosure deals with a peripheral arrangement for a host computer. The peripheral arrangement includes a peripheral card that has a PCMCIA compliant interface that may be generally and advantageously employed when, among others, the peripheral arrangement includes independent functionality, such as may be present if a separate power supply and controller (CPU) is included with the peripheral arrangement. The preferred embodiment is a peripheral card that exhibits an independent and dependent operating state and has an interface function that is coupled to the peripheral card. The interface function is arranged and constructed to couple the peripheral card to the host computer over the PCMCIA compliant interface and initiate a dependent operating state at the peripheral card when inserted in a host computer that is or is subsequently powered up. The interface function that is coupled to the peripheral card during the dependent operating state, initiates an independent operating state when the peripheral card is removed or the host computer is powered down.

25 A preferred embodiment in accordance with the instant invention will be further explained with reference to the Figures, in which FIG. 1 is a block diagram of a host computer (101) and a peripheral arrangement (120) suitable for employing a preferred embodiment in accordance with the instant invention. Depicted in
30 FIG. 1 is the host computer (101) having a PCMCIA slot interface integrated circuit (103) or the like and a PCMCIA connector (105). The peripheral arrangement (120) includes a peripheral card (109) having a PCMCIA interface logic (121), a voltage detector (123), a CPU (125), a power supply (127), a radio transceiver (128), a battery (129), and a
35 PCMCIA connector (132).

The peripheral arrangement (120) is coupled, interfaced, or connected to the host computer (101) by plugging the PCMCIA connector (132) of the peripheral card (109) into the PCMCIA connector (105) of the host computer (101). All these elements (121), (123), (125), (127), (128), (129), and (132) of the peripheral arrangement (120) may be physically located on one PCMCIA compliant or consistent card or the PCMCIA connector (132) may be physically separated from the peripheral card (109) with the physical connection provided by some mechanism, such as a cable, connecting the two. The host computer (101) can be any general purpose computer that includes functionally and logically as well as, preferably, physically a PCMCIA interface that operates according to the PCMCIA standards. The preferred embodiment of the instant invention is considered to be consistent or compliant with the PCMCIA standards and defined PCMCIA interfaces and ports, provided it operates at least in part in accordance with the PCMCIA interface and transparently to the host computer's hardware, operating system software, or other attributes.

In any event the preferred embodiment of the first peripheral card (109), includes, all inter coupled as depicted, a controller, preferably, a central processing unit CPU (125) with associated RAM and ROM, such as a Motorola MCM68300 series microprocessor, a radio transceiver (128) that is arranged to transceive data over a communications medium all as well known in the art, a power supply (127) and a power source, preferably, battery (129) such as NiCAD or 9 volt alkaline or lead acid, that is coupled to the power supply (127). Circuitry, well known, in the power supply (127) allows the CPU (125) to detect the status of the power supply (127) in order to determine the operating state of the peripheral card (109).

In the preferred embodiment whenever the peripheral card (109) is disconnected, decoupled, or pulled out of the host computer (101) by disengaging the PCMCIA connector (105) from the PCMCIA connector (132) or when the host computer's PCMCIA slot interface (103) is powered down while the peripheral arrangement (120) is inserted, the PCMCIA will initiate an independent operating state as described below.

When the PCMCIA power supply line, PCMCIA5V (131) drops below a preset voltage, the voltage detector (123) will deassert the PVD signal (133), which will in turn cause a CPU interrupt signal, GPINT (221) to be generated. The CPU, upon receiving the interrupt, determines the current state of the PVD signal, which can be read as a bit in the PCMCIA interface logic (121). The CPU, having determined that PVD is unasserted, then initiates an independent operating state. At the same time, the deassertion of the PVD signal (133) causes the first register set (201) to be cleared to a default state and held in that default state until the card is reinserted into a powered PCMCIA slot. This ensures that the PCMCIA interface will operate in memory only mode (as opposed to I/O mode) when the card is reinserted into a PCMCIA slot regardless of the interface mode established when the card was removed from the slot.

Consequently, when the card is reinserted or the host computer's PCMCIA slot is powered up, the PCMCIA card will initiate a dependent operating state based on the assertion of the PVD signal. When the PCMCIA power supply line, PCMCIA5V (131) rises above a preset voltage, the voltage detector (123) will assert the PVD signal (133), which will in turn cause a CPU interrupt signal, GPINT (221) to be generated. The CPU, upon receiving the interrupt, determines the current state of the PVD signal, which can be read as a bit in the PCMCIA interface logic (121). The CPU, having determined that PVD is asserted, then initiates a dependent operating state.

In order to avoid the phenomenon of unnecessarily resting circuitry, the PCMCIA card uses four reset signals, each of which resets a specific domain of circuitry. The P_RESET (135) signal originating from the PCMCIA host computer (101) and the PVD signal (when unasserted) primarily reset those circuits which are directly controlled by the PCMCIA host. The C_RESET circuit primarily resets those circuits which are controlled by the integral CPU (125). The fourth reset signal, power on reset, POR (137), originates from the on-board power supply and acts as a global reset of all circuits on the PCMCIA card. POR is asserted (active low) whenever the output of the on-board

power supply is below the minimum operating voltage for the PCMCIA card.

FIG. 2 is a detailed block diagram of the peripheral card of FIG.1. The interface function or PCMCIA interface logic (121) contains three
5 major functional blocks, a first set of registers or PCMCIA registers (201), a second set of registers or CPU registers (203), and a communications block (205) having a third set of registers (206).

The first set of register (201) contains a plurality of registers which can be read and written through the PCMCIA interface via the
10 PCMCIA read and write signals 299, 297 but which may only be read through the CPU interface via CPU read 295. The first set of registers is reset by any one of three reset conditions each coupled through OR gate 211, the PRESET signal (135) being asserted, the POR, active low, signal (137) being asserted or the PVD signal (133) being unasserted. The
15 second set of registers (203) contains a plurality of registers which can be read and written through the CPU interface via CPU read and write 295, 293 but which may only be read through the PCMCIA interface via PCMCIA read 299. The second set of registers is reset by either the CRESET, active low, signal (139) or the POR, active low, being asserted.
20 The communication block (205) contains a third set of registers (206) and their associated logic such as FIFO memory registers and control logic registers. The FIFO memory registers are used to buffer data from the PCMCIA interface to the CPU interface and to buffer data from the CPU interface to the PCMCIA interface. The communications block
25 (205) is reset by any one of the four reset conditions each as coupled through OR gate 215, the PRESET signal (135) being asserted, the POR, active low, signal (137) being asserted, CRESET, active low, signal (139) being asserted, or the PVD signal (133) being unasserted.

As previously stated, in order to avoid the phenomenon of
30 unnecessarily resetting circuitry, the PCMCIA card uses the four reset signals as described, each of which resets a specific domain of circuitry.

The host computer will assert the P_RESET signal (135) whenever it wishes to place the card into a default condition, usually
whenever a new card is inserted into the slot, or when the host
35 computer itself is reset. The assertion of the P_RESET signal (135)

resets the first set of registers or PCMCIA registers (201), and the third set of registers (205) associated with the interface function or PCMCIA interface logic (121). This causes those registers associated with the card interface mode to be reset to memory only access as well as resetting
5 any other registers which had been previously altered by the PCMCIA host, and clears the communications block in preparation for a new communications session.

The PCMCIA interface logic (121) further includes a second set of registers or CPU registers (203) coupled to the integral CPU (125). The
10 integral CPU (125) asserts the CRESET* (where '*' signifies active low) signal whenever it wishes to place the card into a default condition, usually as the result of a software reset, a watchdog timer expiration, or to recover from an error condition. The CRESET* assertion resets the second set of registers and the third set of registers (205) coupled to the
15 CPU (125). This causes all registers which could have been altered by the CPU to be reset, and clears the communications block in preparation for a new communications session.

The assertion of the POR* signal (137) resets the first set of registers, the second set of registers, and the communications block in
20 order to completely reset the PCMCIA interface logic (121) after the power supply output is stable above the minimum operating voltage. Referring to figure 1, the POR* signal (137) is coupled to the CRESET* signal (139) via a diode (141) in order to allow the POR* signal to also reset the CPU (125) and the radio transceiver (128).

25 The PVD signal (133) de-assertion resets the first set of registers (201) and the third set of registers (205). This causes those registers associated with the card interface mode to be reset to memory only access as well as resetting any other registers which had been previously altered by the PCMCIA host, and clears the communications
30 block in preparation for a new communications session when the PCMCIA card is reinserted into a powered PCMCIA slot.

FIG. 3 is flowchart diagram of the steps performed at the peripheral card for determining whether the peripheral card is in a
35 dependent or independent operating state. Beginning with START

block 302, flow proceeds to block 304 where the power to the card is turned on by the power switch on the card. This action causes the on-board power supply to generate a power-on reset which resets all circuit on the card. During the card initialization, at block 306, the integral
5 CPU checks if there is power on the PCMCIA interface by examining the PCMCIA Voltage Detect (PVD) signal. If PVD is asserted; i.e. PVD = 1, the CPU places the card in a dependent operating state at block 308; otherwise the CPU places the card in an independent operating state at block 314.

10 While the card is in an dependent operating state, the interface circuit monitors the PCMCIA power line. If the card is removed from the socket or power is removed from the socket, then PVD = 0 at block 316 and a delta PVD interrupt is generated to the integral CPU at block 318.

15 Similarly, while the card is in an independent operating state, the interface circuit monitors the PCMCIA power line. At block 310, if the card is placed in socket and power is applied to the socket, then PVD = 1 at block 312 and a delta PVD interrupt is generated to the integral CPU at 320.

20 Whenever the CPU receives a delta PVD interrupt, the integral CPU checks if there is power on the PCMCIA interface by examining the PCMCIA Voltage Detect (PVD) signal. If PVD is asserted; i.e. PVD = 1, the CPU places the card in a dependent operating state; otherwise the CPU places the card in an independent operating state.

25 Those skilled in the art will recognize that the instant invention provides a peripheral card with independent functionality that is capable of operating in a independent state when de coupled from a host computer and in a dependent state when coupled to the host computer. Furthermore, the peripheral card may alternatively or
30 additionally be arranged to operate in conjunction with the host computer over a PCMCIA compliant interface.

It will also be apparent to the skilled that the disclosed invention may be modified in numerous ways and may assume many
35 embodiments other than the preferred form specifically set out and described above.

An alternate embodiment of the present invention would not require a voltage detection scheme, as used in a preferred embodiment and described above, but instead would use watchdog timers. If after a predetermined time period, the host computer has not interacted with the PCMCIA card, it would be assumed by the PCMCIA card that it was out of the socket. The CPU on the PCMCIA card would place the card into a independent operating mode. Subsequently, if communications with the host processor is restored, the CPU on the PCMCIA card would resume a dependent operating mode.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

Claims

1. A PCMCIA card having independent functionality and
alternatively arranged to operate in conjunction with a host computer,
5 comprising in combination:
a peripheral apparatus having an integral CPU, a power source,
and a power supply and exhibiting an independent operating state;
an interface function integral with and coupled to said
10 peripheral apparatus, said interface function arranged and constructed
to couple said peripheral apparatus to the host computer over a
PCMCIA compliant interface and initiate a dependent operating state at
said peripheral apparatus.
- 15 2. The PCMCIA card of claim 1, wherein said peripheral apparatus
further includes a voltage detector operating to assert a PCMCIA
voltage detect (PVD) signal, said integral CPU initiating said dependent
operating state at said peripheral apparatus, responsive to said PVD
signal.
- 20 3. The PCMCIA card of claim 1, wherein said interface function
further includes a first set of registers associated with said PCMCIA card
coupled to said host computer over said PCMCIA compliant interface,
said host computer operating to assert a PCMCIA reset (PRESET) signal
25 to reset said first set of registers.
4. The PCMCIA card of claim 1, wherein said interface function
further includes a second set of registers coupled to said integral CPU,
said integral CPU operating to assert a CPU reset (CRESET) signal to
30 reset said second set of registers.
5. The PCMCIA card of claim 4, wherein said interface function
further includes said communications block coupled to said integral
CPU, said integral CPU operating to assert the CPU reset (CRESET)
35 signal to reset the communications block.

6. The PCMCIA card of claim 1, wherein the peripheral apparatus further includes a radio transceiver.
- 5 7. The PCMCIA card of claim 2, further comprising a first status bit being set by an assertion of said PVD signal and being readable by said CPU.
- 10 8. The PCMCIA card of claim 1, wherein said power supply asserts a power-on reset (POR) signal, responsive to a predetermined voltage level, said power-on reset signal resets all circuitry on said PCMCIA card.
- 15 9. A peripheral card having an integral CPU and power supply, the peripheral card including an interface function having a first set registers and a second set of registers coupled to a communications control block having a first set of FIFO registers and a second set of FIFO registers and a set of control registers, the interface function arranged to operate in conjunction with a host computer over a
- 20 PCMCIA compliant interface, a method including the steps of:
- exhibiting a dependent operating state at the peripheral card when operating in conjunction with the host computer; and
- initiating a independent operating state at said peripheral card.
- 25 10. The method of claim 9 further including a step of setting a flag in the interface function by an de-assertion of the PVD signal in order to initiate the independent operating state at said peripheral card.

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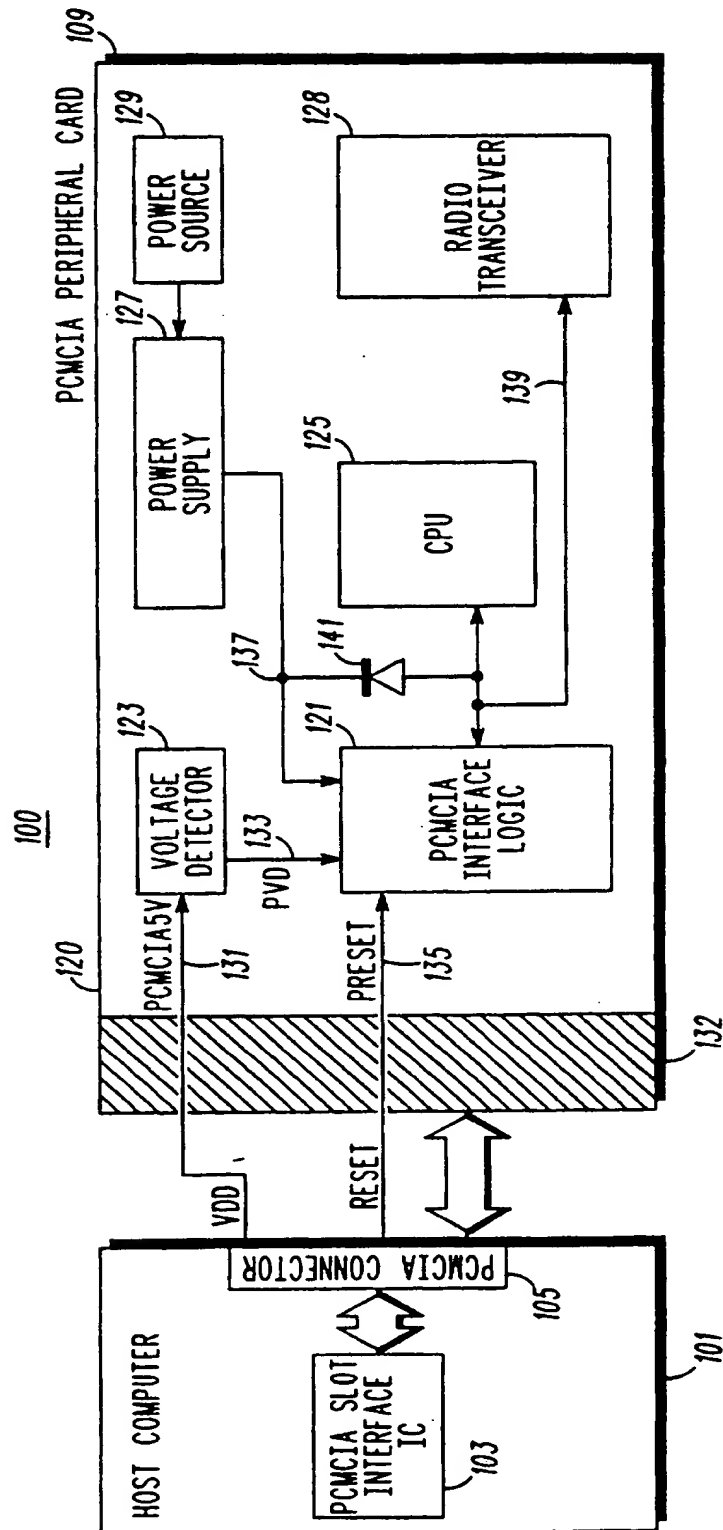
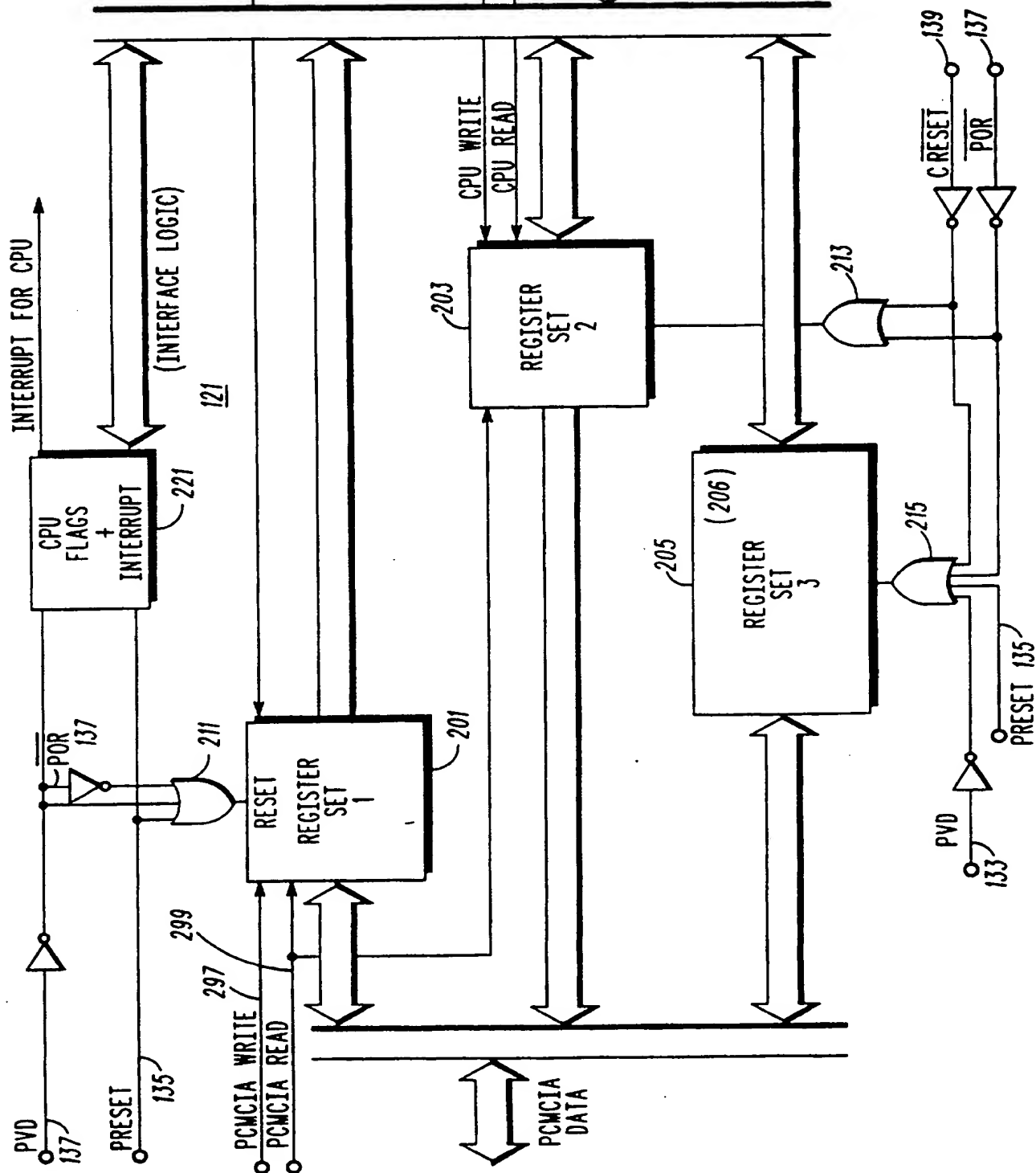


FIG. 1

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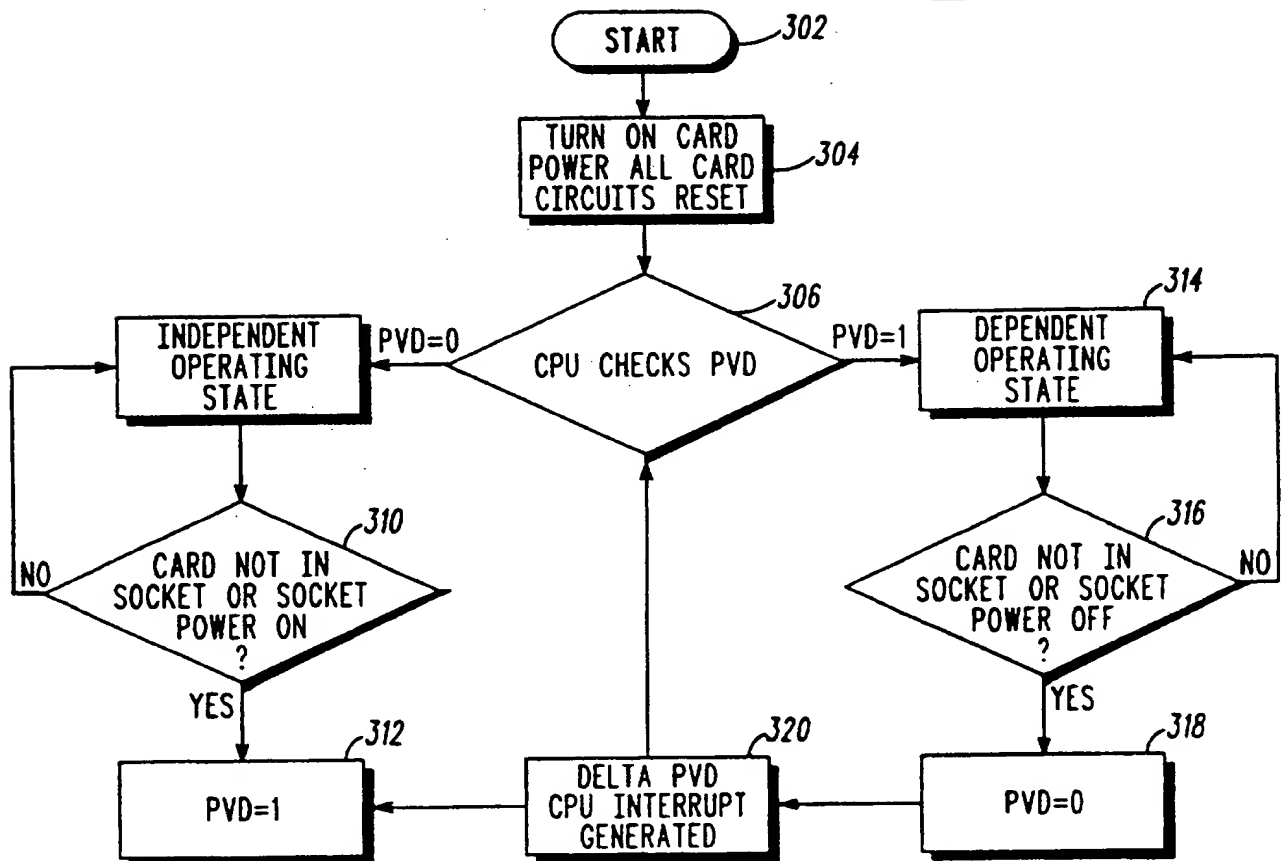
FIG. 2



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FIG. 3

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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G06K13/00, 13/14

US CL : 395/500, 395/325

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

A.P.S.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,365,221 (FENNEL ET AL) 15 November 1994, See figs. 3 and 5, col. 1, lines 11-53, col. 2, lines 9-38.	1-10
Y,E	US, A, 5,455,505 (LAPLACE ET AL) 03 October 1995, See figs. 3-5, col. 2, lines 27-51 and claims 1 and 7.	1-10
A	US, A, 5,334, 046 (BROUILLETE ET AL) 02 August 1994, See the entire document.	1-10
A	US, A, 5,334,030 (BRILLIOTT) 02 August 1994, See the entire document.	1-10

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,E	US, A, 5,451,933 (STRICKLIN ET AL) 19 September 1995, See figs. 5 and 6, col. 1, lines 15-68, col. 2, lines 1-20, 45-62, col. 3, lines 14-56, col. 4, 17-58, col. 5, lines 11-61.	1-10